Module 8: Op-Amp Applications, Active Filters, and Data Converters - Comprehensive Edition

Welcome to Module 8! This module builds upon our foundational understanding of operational amplifiers (op-amps) and delves into a wide array of practical and essential applications that leverage the unique characteristics of these versatile devices. We will begin by reviewing the fundamental amplifier configurations, reinforcing their principles and common uses. Following this, we will explore more advanced op-amp based circuits, including integrators, differentiators, precision rectifiers, and Schmitt triggers, understanding their operation, design considerations, and inherent limitations.

The module then transitions into the fascinating world of **active filters**, where op-amps enable us to create sophisticated frequency-selective circuits without relying on bulky inductors. We will explore the advantages of active filters and provide detailed design guidelines for various types, including low-pass, high-pass, band-pass, and band-stop (notch) filters, focusing on first and second-order Butterworth implementations.

The latter part of the module is dedicated to **data converters**, which bridge the critical gap between analog and digital worlds. We will systematically examine the principles and architectures of various Digital-to-Analog Converters (DACs) and Analog-to-Digital Converters (ADCs), discussing their internal workings and key performance parameters such as resolution, linearity, and sampling rate. Finally, we will introduce the concept of **switched capacitor circuits**, understanding their basic operation and their growing importance in modern integrated circuit design for applications like filters and gain stages. This module aims to provide you with a robust understanding of these advanced op-amp applications and their crucial role in contemporary electronic systems.

8.1 Review of Basic Op-Amp Applications

Operational amplifiers, with their high open-loop gain, high input impedance, and low output impedance, are the workhorses of analog circuit design. When combined with negative feedback, they can be configured to perform a wide variety of precise functions. This section reviews the most fundamental and widely used op-amp configurations, which serve as building blocks for more complex circuits. We will assume ideal op-amp characteristics for simplicity in deriving the gain equations.

Ideal Op-Amp Assumptions (for review):

- Infinite open-loop voltage gain ($A \to \infty$)
- Infinite input impedance ($Z_{in} \to \infty$), meaning zero input current into op-amp terminals ($I_+ = I_- = 0$)
- Zero output impedance ($Z_{out} \to 0$)

- Zero input offset voltage ($V_{offset}=0$), implying $V+=V-$ (virtual short concept)

1. Inverting Amplifier

The inverting amplifier provides a voltage gain while inverting the phase of the input signal. It uses **Voltage Shunt Feedback**.

- **Configuration:** The non-inverting (+) input is grounded. The input signal (V_{in}) is applied to the inverting (-) input through an input resistor (R_{in}). A feedback resistor (R_f) connects the output (V_{out}) to the inverting (-) input.
- **Derivation of Voltage Gain (A_v):**
    - **Virtual Ground:** Since $V+=0$ V and $V+=V-$ (virtual short), then $V-=0$ V. The inverting input is at a "virtual ground."
    - **Input Current (I_{in}):** Current through R_{in} is $I_{in}=(V_{in}-V-)/R_{in}=(V_{in}-0)/R_{in}=V_{in}/R_{in}$.
    - **Feedback Current (I_f):** Due to infinite input impedance, no current flows into the op-amp's inverting terminal. Therefore, all of I_{in} must flow through R_f towards the output. So, $I_f=I_{in}$.
    - **Output Voltage (V_{out}):** The output voltage is related to the current through R_f and the voltage at $V-$. $V_{out}=V--I_fR_f=0-I_{in}R_f$.
    - **Substitute and Solve:** Substitute I_{in} from step 2: $V_{out}=-(V_{in}/R_{in})R_f$. Thus, the closed-loop voltage gain is: $A_v=\frac{V_{out}}{V_{in}}=-\frac{R_f}{R_{in}}$
- **Key Characteristics:**
    - **Phase Inversion:** The negative sign indicates a 180-degree phase shift.
    - **Input Impedance:** Approximately R_{in}.
    - **Output Impedance:** Very low (approaching 0 Ω).
- **Numerical Example:** Design an inverting amplifier with a gain of -10. If $R_{in}=10$ kΩ, then $R_f=A_v\times R_{in}=10\times 10$ kΩ$=100$ kΩ. So, use $R_f=100$ kΩ.

2. Non-Inverting Amplifier

The non-inverting amplifier provides a voltage gain without inverting the phase of the input signal. It uses **Voltage Series Feedback**.

- **Configuration:** The input signal (V_{in}) is applied directly to the non-inverting (+) input. The feedback network consists of R_f connected from output to the inverting (-) input, and R_g connected from the inverting (-) input to ground.
- **Derivation of Voltage Gain (A_v):**
    - **Virtual Short:** Since $V+=V_{in}$ and $V+=V-$ (virtual short), then $V-=V_{in}$.
    - **Voltage Divider Action:** The feedback network (R_f and R_g) acts as a voltage divider for the output voltage. The voltage at $V-$ is the voltage across R_g. $V-=V_{out}\times\frac{R_g}{R_g+R_f}$
    - **Equate and Solve:** Substitute $V-=V_{in}$ into the equation from step 2: $V_{in}=V_{out}\times\frac{R_g}{R_g+R_f}$ Rearrange to find A_v: $A_v=\frac{V_{out}}{V_{in}}=\frac{R_g+R_f}{R_g}=1+\frac{R_f}{R_g}$
- **Key Characteristics:**

    - **No Phase Inversion:** Output is in phase with the input.
    - **Input Impedance:** Extremely high (approaching ∞ Ω), ideal for voltage sources.
    - **Output Impedance:** Very low (approaching 0 Ω).
- **Numerical Example:** Design a non-inverting amplifier with a gain of 5. If Rg=5 kΩ, then 5=1+Rf/5 kΩ, which means 4=Rf/5 kΩ. So, Rf=20 kΩ.

3. Voltage Follower (Unity Gain Buffer)

The voltage follower is a special case of the non-inverting amplifier with a fixed gain of 1. It is primarily used for **impedance buffering**.

- **Configuration:** The input signal (Vin) is applied to the non-inverting (+) input. The output (Vout) is connected directly back to the inverting (-) input (equivalent to Rf=0 and Rg→∞ in the non-inverting configuration).
- **Derivation of Voltage Gain (Av):**
    - **Virtual Short:** Since V+=Vin, then V−=Vin.
    - **Direct Feedback:** Vout is directly connected to V−. Therefore, Vout=V−.
    - **Substitute and Solve:** Vout=Vin. Thus, Av=VinVout=1.
- **Key Characteristics:**
    - **Unity Gain:** Output voltage equals input voltage.
    - **Extremely High Input Impedance:** Makes it suitable for connecting to high-impedance sources (e.g., sensor outputs) without loading them.
    - **Extremely Low Output Impedance:** Makes it suitable for driving low-impedance loads (e.g., long cables, speakers) without significant signal degradation.
- **Numerical Example:** An audio signal source with a 1 MΩ internal resistance needs to drive an amplifier with a 10 kΩ input impedance. Placing a voltage follower between them ensures the signal source is not loaded down, as the voltage follower's input impedance (ideally infinite) draws negligible current, and its low output impedance (ideally zero) efficiently drives the 10 kΩ load.

4. Summing Amplifier (Adder)

The summing amplifier produces an output voltage that is a weighted sum of multiple input voltages. It is a variation of the **inverting amplifier**.

- **Configuration:** Multiple input resistors (R1,R2,…,Rn) are connected from respective input voltages (V1,V2,…,Vn) to the inverting (-) input. A feedback resistor (Rf) connects the output (Vout) to the inverting (-) input. The non-inverting (+) input is grounded.
- **Derivation of Output Voltage:**
    1. **Virtual Ground:** V−=0 V.
    2. **Current Summation at Virtual Ground:** Due to the virtual ground and infinite input impedance of the op-amp, the sum of currents flowing into the inverting node must be zero (Kirchhoff's Current Law). The currents flowing *towards* the node from inputs are I1=V1/R1, I2=V2/R2, etc. The current flowing *away* from the node through Rf is If=(0−Vout)/Rf=−Vout/Rf.

$I1+I2+\cdots+In+If=0$
$R1V1+R2V2+\cdots+RnVn-RfVout=0$

3. **Solve for Vout:**
$RfVout=R1V1+R2V2+\cdots+RnVn$
$Vout=-Rf(R1V1+R2V2+\cdots+RnVn)$

- **Special Case: Averaging Amplifier:** If $R1=R2=\cdots=Rn=R$ and $Rf=R/n$, then $Vout=-(V1+V2+\cdots+Vn)/n$, producing the average of the input voltages (with inversion).
- **Numerical Example:** Design a summing amplifier that outputs $Vout=-(2V1+0.5V2)$. Let $Rf=10\ k\Omega$. From the formula, $Vout=-Rf(V1/R1+V2/R2)$. Comparing coefficients: $Rf/R1=2\Rightarrow R1=Rf/2=10\ k\Omega/2=5\ k\Omega$. And $Rf/R2=0.5\Rightarrow R2=Rf/0.5=10\ k\Omega/0.5=20\ k\Omega$. So, $R1=5\ k\Omega$, $R2=20\ k\Omega$, and $Rf=10\ k\Omega$.

8.2 Op-Amp Based Circuits

Beyond basic amplification and summation, op-amps can be configured to perform a range of complex mathematical and signal conditioning operations. This section delves into some of these advanced applications.

1. Integrator and Differentiator

These circuits perform mathematical operations (integration and differentiation) on the input signal, typically useful in control systems, wave shaping, and analog computing.

a) Integrator

An op-amp integrator produces an output voltage proportional to the time integral of the input voltage.

- **Configuration:** An input resistor (Rin) connects the input signal (Vin) to the inverting (-) input. A feedback capacitor (Cf) connects the output (Vout) to the inverting (-) input. The non-inverting (+) input is grounded.
- **Principle of Operation:** The capacitor Cf is placed in the feedback path. Due to the virtual ground at V−, the input current $Iin=Vin/Rin$. This current flows through Cf (as no current enters the op-amp). The voltage across a capacitor is the integral of the current flowing through it. Since Vout is essentially the voltage across Cf (relative to virtual ground), the output is the integral of the input current, and thus, the integral of the input voltage.
- **Output Voltage Formula:**
$Vout(t)=-RinCf1\int Vin(t)dt$
The negative sign indicates phase inversion. The term RinCf is the integration time constant.
- **Limitations and Practical Considerations:**
    - **DC Gain:** An ideal integrator has infinite DC gain (since a capacitor acts as an open circuit to DC). This causes any DC offset in the input or input bias currents to be integrated and eventually drive the output to saturation (the power supply rails).
    - **Practical Solution (Leakage Resistor):** To prevent saturation due to DC, a large resistor (Rleak) is often placed in parallel with Cf. This resistor provides

a DC path for the feedback, effectively limiting the DC gain to $-R_{leak}/R_{in}$, transforming the integrator into a low-pass filter with a very low cutoff frequency.
    - **Frequency Response:** An ideal integrator has a gain that decreases with frequency at -20 dB/decade. At high frequencies, the gain can become too low, and noise can be amplified.
    - **Input Bias Current:** Input bias currents from the op-amp can also charge the capacitor, leading to output drift. Use op-amps with low input bias current (e.g., FET-input op-amps).
- **Applications:** Analog computers, signal generation (ramp, triangle waves from square waves), waveform shaping, filter design.

b) Differentiator

An op-amp differentiator produces an output voltage proportional to the time derivative (rate of change) of the input voltage.

- **Configuration:** An input capacitor (Cin) connects the input signal (Vin) to the inverting (-) input. A feedback resistor (Rf) connects the output (Vout) to the inverting (-) input. The non-inverting (+) input is grounded.
- **Principle of Operation:** The input current Iin through Cin is $I_{in}=C_{in}\frac{dV_{in}}{dt}$. This current flows through Rf. The output voltage is related to this current by $V_{out}=-I_{in}R_f$.
- **Output Voltage Formula:**
  $V_{out}(t)=-R_fC_{in}\frac{dV_{in}(t)}{dt}$
  The term R_fC_{in} is the differentiation time constant.
- **Limitations and Practical Considerations:**
    - **Noise Amplification:** A differentiator's gain *increases* with frequency at +20 dB/decade. This means it significantly amplifies high-frequency noise components present in the input signal, leading to a noisy output. This is its most significant limitation.
    - **Stability Issues:** The increasing gain at high frequencies can also lead to instability or oscillations.
    - **Practical Solution (Input Resistor):** To limit noise amplification and improve stability, a small resistor (Rlimit) is often placed in series with the input capacitor. This creates a high-frequency pole, limiting the gain at higher frequencies and transforming the differentiator into a high-pass filter with a controlled cutoff frequency.
- **Applications:** Edge detection, pulse shaping, rate-of-change detection in control systems.

2. Precision Rectifier (Active Rectifier)

Unlike passive diode rectifiers that suffer from a significant voltage drop (typically 0.7 V for silicon diodes), a precision rectifier uses an op-amp to effectively eliminate the forward voltage drop, allowing rectification of very small AC signals.

- **Principle:** The op-amp is configured such that its very high gain compensates for the diode's forward voltage drop. The diode is placed within the feedback loop or output path.
- **Half-Wave Precision Rectifier (Non-Inverting):**
    - **Configuration:** A diode (D1) is placed in series with the output of the op-amp, leading to the load. Another diode (D2) can be used in reverse across the feedback path. The feedback resistor (Rf) connects the output (after D1) to the inverting (-) input. Rin connects input to the inverting input.
    - **Positive Input Cycle:** When Vin is positive, the op-amp's output drives positive. The diode D1 turns ON. The op-amp forces Vout (across the load) to be equal to Vin (due to virtual short) regardless of the diode drop, as the op-amp will output the necessary voltage to overcome D1's drop. The output is Vout=Vin (for non-inverting).
    - **Negative Input Cycle:** When Vin is negative, the op-amp's output drives negative. D1 turns OFF. The feedback loop is broken, and the output remains at 0 V. D2 (if present) might turn on to provide a path for the op-amp, preventing saturation.
- **Key Advantage:** Rectifies signals even below the diode's forward voltage drop. Ideal for low-level AC signal processing.
- **Limitations:** Slew rate limitations of the op-amp can affect performance at high frequencies. Op-amp must be able to sink/source current through the diode quickly.
- **Applications:** Peak detectors, absolute value circuits, AC voltmeters, signal conditioning for small AC signals.

3. Schmitt Trigger (Comparator with Hysteresis)

A Schmitt trigger is a comparator circuit that incorporates **hysteresis**, meaning it has two different threshold voltages for switching: one for a rising input signal and another for a falling input signal. This characteristic makes it highly resistant to noise on the input signal.

- **Principle:** Positive feedback is deliberately used to create the hysteresis. The op-amp operates in open-loop (saturated) mode, or with very high gain, driven to its positive or negative saturation limits (+Vsat or −Vsat).
- **Configuration (Non-Inverting Schmitt Trigger):**
    - The input signal (Vin) is applied to the inverting (-) input.
    - The non-inverting (+) input is connected to a voltage divider formed by two resistors (R1,R2) from the output (Vout) to ground. This creates positive feedback.
- **Operation (Non-Inverting Type):**
    - **Upper Threshold Voltage (VUTH):** Assume Vout is initially at −Vsat. The voltage at the non-inverting input (V+) is set by the voltage divider: $V+ = -Vsat \times R2/(R1+R2)$. For the output to switch to +Vsat, the input Vin (at V−) must rise above this threshold. So, $VUTH = -Vsat \times R2/(R1+R2)$.
    - **Lower Threshold Voltage (VLTH):** Once Vout has switched to +Vsat, the voltage at the non-inverting input (V+) becomes $+Vsat \times R2/(R1+R2)$. For the output to switch back to −Vsat, the input Vin (at V−) must fall below this new threshold. So, $VLTH = +Vsat \times R2/(R1+R2)$.

- **Hysteresis Width:** The difference between the upper and lower threshold voltages: Hysteresis=VUTH−VLTH. This provides a "dead zone" that prevents spurious switching due to noise.
- **Advantages:**
    - **Noise Immunity:** The primary advantage. Small noise fluctuations on the input signal will not cause multiple false output transitions as long as they stay within the hysteresis band.
    - **Clean Output Transitions:** Produces sharp, clean square wave outputs, regardless of the input signal's rise/fall time.
    - **Debouncing:** Can be used for switch debouncing.
- **Applications:** Noise immunity in digital circuits, signal conditioning, waveform generation (square wave from sine wave), level detection with threshold memory.

8.3 Active Filters

Active filters are frequency-selective circuits that use active components (like op-amps or transistors) in conjunction with passive components (resistors and capacitors, but typically no inductors). They are widely used to pass desired frequency bands while attenuating unwanted ones.

Advantages of Active Filters:

1. **No Inductors:** This is a major advantage. Inductors are bulky, heavy, expensive, prone to picking up electromagnetic interference, and difficult to integrate into silicon chips. Active filters achieve frequency selectivity using only resistors and capacitors, which are much easier to implement, especially in integrated circuits.
2. **Gain and Isolation:** Active filters can provide gain within the passband, unlike passive filters which always have a gain less than or equal to one. The active element (op-amp) also provides isolation between stages, preventing loading effects.
3. **Flexible Design:** Characteristics like gain, cutoff frequency, and Q-factor (sharpness of cutoff) can be precisely controlled and easily adjusted by varying resistor and capacitor values, often without affecting other parameters.
4. **No Loading Issues:** The high input impedance and low output impedance of op-amps eliminate loading problems between filter stages or between the filter and its source/load.
5. **Small Size and Low Cost:** Due to the absence of inductors and ease of integration, active filters are generally smaller, lighter, and less expensive to manufacture, especially in IC form.

Filter Terminology:

- **Cutoff Frequency (fc or ωc):** The frequency at which the filter's output power is half of the input power, or the voltage gain drops to 1/2  (approximately 0.707) of its maximum passband value (i.e., -3dB point).

- **Order of a Filter:** Determined by the number of reactive components (capacitors, or equivalent RC sections) that contribute to the frequency response. Each order generally contributes a -20 dB/decade roll-off in the stopband.
- **Butterworth Filter:** A type of filter known for its maximally flat passband response and a monotonic roll-off in the stopband. It has no ripples in the passband or stopband. It's a common choice for general-purpose applications where flat response is desired.

1. Low-Pass Filter

A low-pass filter (LPF) allows frequencies below a certain cutoff frequency (fc) to pass through relatively unimpeded while attenuating frequencies above fc.

- **1st Order Butterworth Low-Pass Filter:**
  - **Configuration (e.g., Sallen-Key):** Often implemented with a resistor and capacitor in the forward path and another resistor in the feedback path.
  - **Cutoff Frequency Formula:**
    $f_c = 2\pi RC_1$
    Where R and C are the chosen resistor and capacitor values in the RC section.
  - **Roll-off:** -20 dB/decade (-6 dB/octave) in the stopband.
  - **Design Guidelines:** Choose a capacitor value (e.g., 0.1 µF or 0.01 µF) and then calculate the required resistor value for the desired fc.
- **2nd Order Butterworth Low-Pass Filter:**
  - **Configuration (e.g., Sallen-Key):** Uses two resistors (R1,R2) and two capacitors (C1,C2) to achieve the second order. A non-inverting op-amp configuration is common.
  - **Cutoff Frequency Formula (for R1=R2=R and C1=C2=C):**
    $f_c = 2\pi RC_1$
    This is a common simplification, but for a true Butterworth response, often C1=2C2 or specific ratios of R and C are used to achieve the correct damping factor (2  for 2nd order Butterworth).
  - **Roll-off:** -40 dB/decade (-12 dB/octave) in the stopband.
  - **Design Guidelines:** For a unity-gain 2nd order Butterworth filter, a common approach is to choose C1=2C and C2=C, and set R1=R2=R. Then $f_c = 1/(2\pi RC_1C_2$ ). Using C1=2C2 simplifies to $f_c = 1/(2\pi RC_2^2$ ). A simpler design is to choose R1=R2=R and C1=C2=C, then the gain must be adjusted (e.g., Av=1.586) to achieve the Butterworth response.

Or, for a unity gain, choose R1=R2=R and C1=2C,C2=C, so fc=1/(2πRC). The key is to achieve the correct damping factor.

- **Numerical Example (1st Order LPF):** Design a 1st order LPF with fc=10 kHz. Choose C=0.01 μF. R=1/(2πfcC)=1/(2π×10×103 Hz×0.01×10−6 F)≈1591.5 Ω. Use R≈1.6 kΩ.

2. High-Pass Filter

A high-pass filter (HPF) allows frequencies above a certain cutoff frequency (fc) to pass through while attenuating frequencies below fc.

- **1st Order Butterworth High-Pass Filter:**
  - **Configuration:** Similar to LPF, but R and C positions are swapped (capacitor in series at input, resistor to ground).
  - **Cutoff Frequency Formula:**
    fc=2πRC1
  - **Roll-off:** +20 dB/decade (+6 dB/octave) in the stopband.
- **2nd Order Butterworth High-Pass Filter:**
  - **Configuration:** Uses two capacitors and two resistors, often in a Sallen-Key configuration where the capacitors are in the series path and resistors are in the shunt path and feedback.
  - **Cutoff Frequency Formula (for R1=R2=R and C1=C2=C):**
    fc=2πRC1
    Again, careful selection of component ratios (e.g., R1=R,R2=R/2) or gain adjustment is needed for true Butterworth.
  - **Roll-off:** +40 dB/decade (+12 dB/octave) in the stopband.
- **Design Guidelines:** Similar considerations as for LPF but with swapped R and C positions.

3. Band-Pass Filter

A band-pass filter (BPF) allows a specific range of frequencies (the passband) to pass while attenuating frequencies both below and above this band.

- **Configuration:** Can be designed by cascading a high-pass filter and a low-pass filter (HPF followed by LPF), or by using specialized multiple-feedback or state-variable filter circuits. The cutoff frequency of the HPF must be lower than the cutoff frequency of the LPF.
- **Key Parameters:**
  - **Center Frequency (fo):** The frequency at which the filter has maximum gain.
  - **Bandwidth (BW):** The difference between the upper (fH) and lower (fL) 3dB cutoff frequencies (BW=fH−fL).
  - **Quality Factor (Q):** A measure of the filter's selectivity. Q=fo/BW. A higher Q means a narrower bandwidth and sharper selectivity.
- **Formulas (simplified, for common BPF architectures like Multiple Feedback):**
  - fo=2πRC1 (for certain configurations where R and C are common)
  - BW and Q depend on component ratios in the specific circuit.

- **Design Guidelines:** Often involves iterative design or using tables/software for complex Q factors. For simple cascaded HPF-LPF, ensure $f_{c,HPF} < f_{c,LPF}$.

4. Band-Stop Filter (Notch Filter)

A band-stop filter (BSF), also known as a notch filter, attenuates a specific narrow range of frequencies while allowing all other frequencies to pass.

- **Configuration:** Can be implemented by combining a low-pass filter and a high-pass filter in parallel, summing their outputs. The cutoff frequencies of the LPF and HPF are set to overlap to create the notch. Another common circuit is the Twin-T Notch Filter.
- **Key Parameters:**
    - **Notch Frequency (f_{notch}):** The frequency at which maximum attenuation occurs.
    - **Bandwidth (BW):** The width of the attenuated band.
    - **Depth of Notch:** How much attenuation is achieved at the notch frequency.
- **Formulas (simplified for Twin-T):**
    - $f_{notch} = 2\pi RC1$ (for the balanced Twin-T network)
- **Applications:** Eliminating specific interference frequencies, such as 50 Hz or 60 Hz hum from power lines.

8.4 Digital-to-Analog Converters (DACs)

Digital-to-Analog Converters (DACs) are essential interfaces that transform a digital code (binary representation) into an equivalent analog voltage or current. They are crucial components in digital audio players, video systems, process control, and arbitrary waveform generators.

General Principle: A DAC essentially takes a binary input (e.g., an 8-bit or 16-bit word) and, based on the value of each bit (0 or 1), produces a corresponding weighted contribution to the analog output.

1. Weighted Resistor DAC

- **Principle:** Uses a summing amplifier (op-amp in inverting configuration) with a set of input resistors, each chosen to be inversely proportional to the weight of its corresponding binary bit.
- **Configuration:** For an N-bit DAC, N resistors ($R, R/2, R/4, \ldots, R/2^{N-1}$) are connected from switches (controlled by binary bits) to the inverting input of an op-amp. The switches connect either to a reference voltage (V_{ref}) for a '1' bit or to ground for a '0' bit. A feedback resistor (R_f) is connected between the output and the inverting input.
- **Output Voltage Formula (for N bits, b_0 is LSB, b_{N-1} is MSB):**
  $V_{out} = -V_{ref}\left(\frac{b_{N-1}}{R}R_f + \frac{b_{N-2}}{2R}R_f + \cdots + \frac{b_0}{2^{N-1}R}R_f\right)$
  Often, $R_f = R$ is chosen for simplicity. Then:
  $V_{out} = -V_{ref} \sum_{i=0}^{N-1} b_i 2^{i-(N-1)}$
  Alternatively, if $R_f = R/2^N$, then the maximum output can be V_{ref}.

- **Advantages:** Conceptually simple.
- **Disadvantages:**
    - **High Precision Resistors:** Requires a wide range of highly precise resistors (e.g., for 10 bits, resistors range from R to R/512). This is difficult and expensive to manufacture, especially for high resolution.
    - **Input Impedance Variation:** The effective input impedance seen by the op-amp varies with the digital input, which can affect performance.
    - **Bit Switching Time:** Different bit current paths can lead to varying switching speeds, causing glitches.
- **Numerical Example (3-bit Weighted Resistor DAC):** Vref=5 V, Rf=10 kΩ. Let's design it such that RMSB=10 kΩ (so it corresponds to R in the formula). RMSB=R. Rbit−1=R/2=5 kΩ. RLSB=R/4=2.5 kΩ. For input code 101 (MSB, 0, LSB), Vout=−5 V×(10 kΩ1×10 kΩ+5 kΩ0×10 kΩ+2.5 kΩ1×10 kΩ)=−5 V×(1+0+4)=−25 V. (Note: This example shows the *principle*. In practice, the resistor ratios are chosen such that RMSB is the smallest resistance RMSB=R/2N−1 and RLSB=R. Then the formula is Vout=−Vref×(bN−1+bN−2/2+⋯+b0/2N−1).) A more practical example where Rf=R: Let R=10 kΩ for MSB (so 2N−1 term is R), Rf=10 kΩ.
  Vout=−Vref×(bN−1+bN−2/2+⋯+b0/2N−1). For 3 bits, N=3. b2,b1,b0.
  Vout=−Vref×(b2+b1/2+b0/4). If digital input is 101 (b2=1,b1=0,b0=1) and Vref=5V:
  Vout=−5 V×(1+0/2+1/4)=−5 V×(1+0.25)=−5 V×1.25=−6.25 V.

2. R-2R Ladder DAC

- **Principle:** Overcomes the resistor precision problem of the weighted resistor DAC by using only two resistor values: R and 2R. This makes it much easier to manufacture accurately.
- **Configuration:** Consists of a ladder network of resistors, where each "rung" consists of a 2R series resistor and an R shunt resistor. Each bit position controls a switch that connects its corresponding 2R resistor to either the reference voltage (Vref) or ground. The output of the ladder is typically connected to the input of an op-amp (as a current-to-voltage converter) or directly to a buffer.
- **Output Voltage Formula (for N bits, b0 is LSB, bN−1 is MSB):** For an op-amp based R-2R ladder (current output fed to op-amp for voltage output), with feedback resistor Rf:
  Vout=−Vref(2RRf)i=0∑N−1bi2i
  Often, Rf is chosen as R or 2R for convenient scaling. If Rf=2R:
  Vout=−Vrefi=0∑N−1bi2i−1
  (This formula implies a normalized Vref and an output range. The general form is Vout=−Vref2NDecimalValue.)
- **Advantages:**
    - **High Precision:** Only requires accurate ratios of R and 2R, which are much easier to achieve in integrated circuit manufacturing.
    - **Constant Input Impedance:** The effective impedance seen by the reference voltage is constant.
- **Disadvantages:** Still requires accurate resistor values, though less diverse.
- **Numerical Example (3-bit R-2R DAC):** Let R=10 kΩ, 2R=20 kΩ, Vref=5 V. Assume the output current is converted to voltage with an op-amp and Rf=20 kΩ. For input code 101 (b2=1,b1=0,b0=1): Decimal Value = 1×22+0×21+1×20=4+0+1=5.

Maximum decimal value for 3 bits = 23−1=7. Vout=−Vref×2NDecimal Value=−5 V×235=−5 V×85=−3.125 V.

3. Resistor String DAC (String DAC)

- **Principle:** Uses a series string of identical resistors to create 2N equally spaced voltage levels from a reference voltage. A digital multiplexer (selector) then chooses one of these voltage levels as the analog output.
- **Configuration:** A voltage reference Vref is applied across a series string of 2N identical resistors. This creates 2N+1 taps, each representing a distinct voltage level. A digital decoder and a multiplexer (often implemented with analog switches) select the appropriate tap based on the input digital code. A buffer op-amp is usually used at the output to provide low output impedance.
- **Advantages:**
    - **Guaranteed Monotonicity:** Always monotonic (output never decreases for an increasing input code), which is crucial for many applications.
    - **Simplicity:** Very simple in concept.
    - **Small Footprint:** Highly suitable for integrated circuits for lower resolutions.
- **Disadvantages:**
    - **Number of Resistors:** Requires 2N resistors for N bits. This becomes impractical for high resolutions (e.g., 10 bits require 1024 resistors, 16 bits require 65,536 resistors).
    - **Switching Speed:** Can be slower for higher resolutions due to large number of switches.
- **Applications:** Commonly used for low-resolution DACs (e.g., 8-10 bits) and often employed as internal DACs within ADCs (e.g., flash ADCs, successive approximation ADCs).

Key DAC Parameters:

- **Resolution:** The smallest change in analog output voltage corresponding to a 1-bit change in the digital input. It is determined by the number of bits (N). A higher number of bits means finer resolution.
  Resolution=2N−1VFS
  Where VFS is the full-scale output voltage.
- **Linearity (Integral Non-Linearity - INL and Differential Non-Linearity - DNL):**
    - **INL:** The maximum deviation of the actual output voltage from the ideal straight line connecting the zero and full-scale outputs.
    - **DNL:** The maximum deviation of the step size between adjacent output codes from the ideal 1 LSB step. Ideally, DNL = 0, meaning all steps are exactly 1 LSB. If DNL > 1 LSB, it can lead to missing codes.
- **Settling Time:** The time required for the analog output to settle to within a specified error band (e.g., ±1/2 LSB) of its final value after a full-scale digital input change. A shorter settling time means a faster DAC.
- **Monotonicity:** A DAC is monotonic if its analog output never decreases when the digital input code increases. This is a crucial property for control systems to avoid oscillations.

- **Output Glitches:** Momentary spikes in the output voltage during transitions, especially when multiple bits change (e.g., from 0111 to 1000). These are often caused by uneven switching times of different bits.

8.5 Analog-to-Digital Converters (ADCs)

Analog-to-Digital Converters (ADCs) perform the inverse operation of DACs: they convert a continuous analog voltage (or current) into a discrete digital code. ADCs are fundamental for interfacing real-world analog signals with digital processors, microcontrollers, and computers.

General Principle: An ADC samples an analog voltage, quantizes it into discrete steps, and then encodes each step into a binary number.

1. Single Slope ADC (Ramp ADC or Integrating ADC)

- **Principle:** Compares the unknown input analog voltage (Vin) with a linearly increasing (or decreasing) ramp voltage. A counter starts when the ramp begins and stops when the ramp voltage equals Vin. The final count is proportional to Vin.
- **Configuration:** Consists of a voltage ramp generator (often an op-amp integrator), a comparator, a counter, and a timing control unit.
- **Operation:**
    - The counter is reset, and the ramp generator starts.
    - The comparator continuously compares Vin with the ramp voltage.
    - When the ramp voltage equals Vin, the comparator output flips, stopping the counter.
    - The final count in the counter is the digital representation of Vin.
- **Advantages:** Relatively simple circuit.
- **Disadvantages:**
    - **Speed:** Very slow, as the conversion time depends on the magnitude of Vin (worst case is for full-scale input).
    - **Accuracy:** Highly dependent on the linearity and stability of the ramp generator and the clock frequency. Susceptible to drift over temperature and time.
- **Applications:** Low-cost, low-speed applications (e.g., digital voltmeters, some sensors).

2. Dual Slope ADC (Dual Ramp ADC)

- **Principle:** An improved integrating type ADC that achieves higher accuracy and linearity by compensating for errors in the ramp generator and clock frequency. It performs two integration phases.
- **Configuration:** Similar to single slope, but with a precision integrator that performs two integrations.
- **Operation:**
    - **Integration of Input:** For a fixed time period (T1), the unknown input voltage (Vin) is integrated, causing the capacitor to charge up. The voltage on the

capacitor at the end of T1 is proportional to Vin×T1. A counter also runs during this phase, counting up to a fixed value.
    - **Integration of Reference:** After T1, the input to the integrator is switched to a fixed negative reference voltage (−Vref). The capacitor then discharges linearly. A second counter starts from zero and counts until the capacitor voltage returns to zero.
    - **Conversion:** The time (T2) taken for the capacitor to discharge to zero is proportional to the peak voltage achieved during the first phase, and thus proportional to Vin. Since VinT1=VrefT2, then Vin=Vref(T2/T1). The count N2 during T2 is the digital output.
- **Advantages:**
    - **High Accuracy and Linearity:** Errors due to capacitor tolerance, clock frequency drift, and integrator gain drift cancel out between the two integration phases.
    - **Excellent Noise Rejection:** Integrates noise over time, providing good rejection of power line hum (if T1 is a multiple of the power line period).
- **Disadvantages:** Very slow conversion time, typically the slowest type of ADC.
- **Applications:** High-precision digital multimeters, instrumentation, weighing scales, sensors where speed is not critical but accuracy is paramount.

3. Successive Approximation ADC (SAR ADC)

- **Principle:** Uses a digital-to-analog converter (DAC) in a feedback loop. It determines the digital output bit by bit, starting from the Most Significant Bit (MSB) down to the Least Significant Bit (LSB), by comparing the DAC's output to the analog input.
- **Configuration:** Consists of a Sample-and-Hold (S/H) circuit, a comparator, a DAC, and a Successive Approximation Register (SAR).
- **Operation (for an N-bit ADC):**
    - The S/H circuit samples and holds the analog input Vin.
    - The SAR sets the MSB (bN−1) of the DAC to '1' and all other bits to '0'.
    - The DAC converts this digital code to an analog voltage (VDAC).
    - The comparator compares Vin with VDAC.
    - If Vin>VDAC, the MSB is kept as '1'; otherwise, it's reset to '0'.
    - The process repeats for the next MSB (bN−2), and so on, for all N bits. Each bit is determined in sequence.
    - After N comparison cycles, the SAR contains the full N-bit digital code.
- **Advantages:**
    - **Good Speed:** Much faster than integrating ADCs, as conversion time is fixed for a given resolution (N clock cycles for N bits).
    - **High Resolution:** Can achieve very high resolutions (up to 24 bits).
    - **Power Efficient:** Generally good power consumption.
- **Disadvantages:** Resolution is inversely proportional to speed (higher bits mean more clock cycles).
- **Applications:** General-purpose data acquisition, industrial control, battery-powered devices, audio, modems.

4. Flash ADC (Parallel ADC)

- **Principle:** The fastest type of ADC. It uses a bank of comparators, each with a unique reference voltage, to simultaneously compare the input analog voltage against all possible quantization levels.
- **Configuration:** Consists of $2N-1$ comparators for an N-bit ADC, a voltage divider (string of resistors) to generate $2N-1$ equally spaced reference voltages, and a priority encoder.
- **Operation:**
    - The analog input voltage (Vin) is simultaneously applied to all comparator inputs.
    - Each comparator has a unique reference voltage, spaced by 1 LSB.
    - All comparators whose reference voltage is below Vin will output a HIGH logic level. All comparators whose reference voltage is above Vin will output a LOW logic level.
    - This creates a "thermometer code" output.
    - A priority encoder converts this thermometer code into a standard N-bit binary output.
- **Advantages:**
    - **Extremely Fast:** Converts in a single clock cycle (parallel operation). Ideal for very high-speed applications.
    - **Simple Operation:** Conceptually straightforward.
- **Disadvantages:**
    - **High Power Consumption:** Many comparators operating simultaneously.
    - **Large Chip Area:** Requires $2N-1$ comparators, which scales exponentially with resolution. Impractical for resolutions above 8-10 bits.
    - **High Cost:** Due to the number of components.
- **Applications:** Video signal processing, radar, high-speed oscilloscopes, digital communications, RF applications.

Key ADC Parameters:

- **Resolution:** The smallest analog voltage change that the ADC can detect and convert into a digital code. Determined by the number of bits (N).
  $\text{Resolution} = \frac{V_{FS}}{2N-1}$
  Where V_{FS} is the full-scale input voltage range.
- **Sampling Rate (Sampling Frequency):** The number of conversions performed per second. A higher sampling rate allows for capture of higher frequency analog signals (Nyquist-Shannon sampling theorem states that sampling rate must be at least twice the highest frequency component of the analog signal).
- **Quantization Error:** The inherent error introduced during the conversion process due to the finite number of discrete digital output levels. It is the difference between the actual analog input value and the closest available digital output level. The maximum quantization error is typically ±1/2 LSB.
- **Conversion Time:** The time it takes for the ADC to complete a single conversion.
- **Linearity (INL and DNL):** Similar to DACs, these specify how accurately the ADC maps analog input to digital output.
    - **INL:** Deviation from the ideal straight line.
    - **DNL:** Deviation of the step size from the ideal 1 LSB. Missing codes occur if DNL > 1 LSB.

- **Signal-to-Noise Ratio (SNR):** A measure of the overall quality of the ADC. For an ideal N-bit ADC, SNR (in dB) ≈6.02N+1.76 dB.

8.6 Switched Capacitor Circuits: Basic Concept and Applications

Switched capacitor (SC) circuits are a revolutionary technique that enables the emulation of resistors using only capacitors and analog switches (typically MOSFETs), along with op-amps. This technique is particularly important in integrated circuit (IC) design, where it is challenging to implement high-precision resistors and bulky inductors.

Basic Concept: Emulating a Resistor

- **The Problem:** In ICs, accurate absolute resistor values are difficult to achieve. However, accurate *ratios* of resistors are much easier. Similarly, accurate capacitor ratios are achievable.
- **The Solution:** Consider a capacitor Csw and two switches (S1,S2) connected to it.
    1. When S1 closes and S2 opens, Csw charges to V1.
    2. When S1 opens and S2 closes, Csw discharges its charge to V2. This process is repeated at a high switching frequency (fclk).
- **Charge Transfer:** In each cycle, a charge Q=Csw(V1−V2) is transferred.
- **Average Current:** The average current flowing between V1 and V2 is the total charge transferred per unit time: Iavg=Q×fclk=Csw(V1−V2)fclk.
- **Equivalent Resistance:** We know that for a resistor, I=(V1−V2)/Req. By equating the two current expressions:
  ReqV1−V2=Csw(V1−V2)fclk
  This yields the equivalent resistance:
  Req=Cswfclk1
  This is the fundamental principle: a resistor can be emulated by a capacitor and two switches clocked at a certain frequency.

Key Advantages of Switched Capacitor Circuits:

1. **Monolithic Integration:** Capacitors and MOSFET switches are easily fabricated on integrated circuits, unlike precise resistors or inductors.
2. **Accuracy and Tunability:** The equivalent resistance (and thus frequency response in filters, or gain in amplifiers) depends on the ratio of capacitors and the clock frequency. Both capacitor ratios and clock frequency can be precisely controlled, allowing for highly accurate and tunable circuits.
3. **Process Independence:** The performance of SC circuits is less sensitive to variations in absolute component values during fabrication, as it relies on ratios.
4. **Low Power Consumption:** In many cases, can operate at very low power.

Applications:

Switched capacitor circuits are widely used in a variety of mixed-signal integrated circuits:

1. **Active Filters:**
    - SC filters can implement high-order, high-performance filters (low-pass, high-pass, band-pass) with precise and tunable cutoff frequencies.
    - The cutoff frequency is directly proportional to the clock frequency, making them easily adjustable.
    - They are prevalent in audio processing, anti-aliasing filters, and communication systems.
2. **Programmable Gain Amplifiers (PGAs):**
    - By replacing resistors in op-amp gain stages with SC equivalent resistors, the gain can be precisely set and easily programmed by changing the clock frequency or capacitor ratios.
    - $Av = -R_{in,eq}R_{f,eq} = -1/(C_{in,sw}f_{clk})1/(C_{f,sw}f_{clk}) = -C_{f,sw}C_{in,sw}$
    - This shows that gain becomes a ratio of capacitances, highly accurate in ICs.
3. **Data Converters (ADCs and DACs):**
    - Switched capacitor techniques are fundamental to the operation of many modern SAR ADCs and sigma-delta ADCs, providing precise charge redistribution and analog summing functions.
    - SC DACs convert digital codes into charge packets, which are then summed to produce an analog output.
4. **Voltage Multipliers/Dividers:** Can generate specific DC voltage levels or ratios using charge pumps.
5. **Analog Memories:** Capacitors can store analog voltages for short periods, enabling functions like sample-and-hold circuits within ADCs.

Numerical Example: Equivalent Resistance of a Switched Capacitor: A switched capacitor circuit uses a capacitor $C_{sw} = 100$ pF and operates with a clock frequency $f_{clk} = 100$ kHz.

Calculate the equivalent resistance (R_{eq}):

$R_{eq} = C_{sw}f_{clk}1 = 100 \times 10^{-12}\ F \times 100 \times 10^{3}\ Hz1$
$R_{eq} = 10 \times 10^{-6}1 = 100{,}000\ \Omega = 100\ k\Omega$

This demonstrates how a small capacitor and a clock signal can emulate a precision resistor value, which is highly advantageous for integrated circuit design.